ABSTRACT OF THE DISCLOSURE

A phase-locked loop has a phase detector that generates a phase difference signal, a circuit that generates a phase-locked loop output signal having a frequency that is a function of the phase difference signal, a frequency divider that receives the phase-locked loop output signal and generates therefrom a divided frequency signal. To substantially reduce variation in the duty cycle of the divided frequency signal, a comparison signal having one half the frequency of the divided frequency signal is generated. This may be performed by configuring a latch to toggle its output state once for every cycle of the divided frequency signal. To compensate for the additional division by two in the feedback path, the phase detector may use a dual-edge triggered latch to generate the phase difference signal so that it represents a phase difference between the reference signal and a signal having twice the frequency of the comparison signal.